REMARKS

Claims 1-11 and 13-28 are pending in this application. By this Amendment, claims 1-4, 7-11, 13, 15, and 17-20 are amended, claim 12 is canceled, and new claims 23-28 are added. Reconsideration of the application and withdrawal of all the rejections of record is respectfully requested for the following reasons.

In response to the Examiner's requirement, a Substitute Specification has been filed with this paper which is more clearly legible than the specification originally filed. The Substitute Specification introduces no new matter into the application. Support for the pending claims can be found throughout the original and substitute specifications, including in the original claims and drawings.

Applicant gratefully acknowledges the indication that claims 8, 9, 18 and 19 would be allowable if rewritten in independent form including all of the limitation of the base claim and any intervening claims. Claims 8, 9, 18, and 19 have been rewritten in this manner. For at least the reasons set forth below, Applicant further submits that all pending claims are in condition for allowance.

In the Office Action, the Examiner objected to claims 3-6 and 13-19 for reciting an abbreviation by itself. By this Amendment, the claims have been amended to recite the full term "excessive bit error ration" along with its abbreviation. Accordingly, withdrawal of objection is respectfully requested. Furthermore, the phrase "repairing duration time" in claim 17 was said to be unclear. Applicant respectfully submits that the phrase error repairing duration time has

clear and definite meaning when read in view of the specification. See, for example, the specification page 13, line 20 and page 17, lines 3-6, wherein the repairing duration time is illustratively disclosed to be an alarm clearing duration time. Based on the foregoing explanations and amendments, withdrawal of objection is respectfully requested.

Claim 1 is rejected under 35 U.S.C.§102(b) as being anticipated by Bullock et al (USPN 5,764,651) (hereinafter Bullock). Because the Bullock patent fails to disclose all the features of claim 1 as amended, the rejection as applied to this claim should be withdrawn.

First, the Bullock patent discloses a method for detecting bit error rate using a window for sampling of error bits in the data stream of an automatic protection switching system for a SONET (synchronous optical network). See column 3, lines 25-62. This method uses a sliding window technique to average the BER. However, Bullock fails to disclose determining an average number of bit errors in the monitored portions of buffer as recited in claim 1. Rather, Bullock discloses averaging the entire window.

Second, the Bullock patent fails to disclose "controlling an alarm based on the average number of bit errors" obtained in the determining step.

Because Bullock fails to teach or suggest at least the features of monitoring a portion of buffers, determining an average number of bit errors in the monitored portion of buffers, and then controlling an alarm based on the computed average for the monitored buffers, it is

respectfully submitted that the Bullock patent can neither anticipate nor render obvious claim 1 or any of its dependent claims.

Claims 1-7, 10-17 and 20-22 are rejected under 35 U.S.C. §102(e) for being anticipated by the Burke et al. (U.S.P.N. 6310,911) (hereinafter Burke). Because Burke fails to disclose all the features of these claims, the Burke patent cannot anticipate the invention as defined in these claims.

The Burke patent discloses two separate bit error rate monitors detecting the presence and/or absence of a particular bit error ratio (BER) and a bit error rate monitor client responsible for reaction to notification from bit error rate monitors. The bit error rate monitors keep track of whether the monitored object is currently detecting a bit error rate. If a new error count sample is received, the value at the tail of the sample queue is removed and subtracted from the total number of errors that have been accumulated over the width of the integration window, also known as sliding window technique. If the new total compared to the parity error count threshold value is less than the threshold, it goes to "less than" state. Otherwise, it goes to "equal to or exceed" state. See column 2, lines 1-62.

Burke also discloses including two error monitors with two different thresholds accordingly, and whenever either of the bit error rate monitors detects a crossing of the parity error count threshold, they inform the bit error monitor client of this crossing. Then, this client considers the current state of both of the monitors and proceeds to raise/clear alarms however

appropriate. See column 3, lines 10-60. In addition, Burke discloses using the simple fixed window technique, the blocked fixed window algorithm, the simple sliding window algorithm, and the exponential sliding window algorithm. All of these window algorithms include either a fixed window size or a fixed block size to monitor the bit error rate.

Claim 1 recites broadly the embodiments of the method of the present invention disclosed in the specification. This method measures the bit error ratio of a transmission system by initializing a plurality of buffers, storing a number of bit errors generated in a transmission during a period of time T in the plurality of buffers, monitoring a portion of buffers among the plurality of buffers for a time period less than T, and determining an average number of bit errors in the monitored portion of buffers.

As noted above, Applicant respectfully submits that Burke fails to disclose at least the feature of monitoring portion of buffers. Burke, rather, discloses monitoring the number of errors that have occurred over a fixed length of time which corresponds to the entire size of its sliding window (see column 7, lines 45-62), not over a portion of that window or as recited for the portion of buffers which are being monitored as recited in claim 1. Burke also fails to disclose determining an average number of bit errors stored in the monitored portion of the buffers, and for then controlling an alarm based on the determined average.

Applicant respectfully submits that claim 1 is allowable over the Burke patent for at least the reasons set forth above. Claims 2-6 depend from claim 1, and are allowable for at least the

same reasons as well as added features and the combination thereof. Withdrawal of the rejection is respectfully requested.

With respect to the rejection of claim 7, Applicant respectfully submits that Burke fails to disclose the claimed feature as amended. As noted above, Burke discloses using various window algorithms including a simple sliding window algorithm. All of these window techniques include either a fixed window size or fixed block size to monitor the bit error rate. See column 10 lines 23-56. Yet, Burke does not disclose monitoring a subset of the plurality of buffers from a current buffer to one of a first and second prescribed buffer as recited in claim 7. Burke also fails to disclose determining an average number of bits errors stored in the subset of buffers. Absent these features, it is respectfully submitted that claim 7 is allowable over Burke.

With respect to the rejection of claim 10, Applicant respectfully submits that Burke fails to disclose many of the claimed features reci ted therein. As noted above, Burke discloses having two error monitors 1, 2 responsible for detecting bit error ratio and monitor 1 detects the presence of 1E-6 whereas monitor 2 detects 1E-7. See column 3, lines 9-32. Yet, Burke does not disclose at least a second error detector to monitor at least a portion of buffers of the plurality of buffers as recited in claim 10.

In view of the foregoing, it is respectfully submitted that Burke does not disclose or suggest the method for measuring the bit error ratio of transmission system, which includes at least a second error detector to monitor at least a portion of buffers of the plurality of buffers.

Accordingly, it is respectfully submitted that claim 10 is allowable for the reasons set forth above. Claims 11-16 depend from claim 10, and are allowable for at least the same reasons as well as added features and the combination thereof. Withdrawal of the rejection is respectfully requested.

With respect to the rejection of claim 17, Applicant respectfully submits that Burke fails to disclose the claimed features as amended. As noted above, Burke discloses this client monitor considers the current state of both of the error monitors and proceeds to raise/clear alarms however appropriate. Yet, Burke does not disclose calculating an average number of bit errors stored in a first subset of sliding window buffers corresponding to the E-BER error generation duration time, or calculating an average number of bit errors stored in a second subset of the sliding window buffers corresponding to the E-BER error repairing duration time.

In view of the foregoing, it is respectfully submitted that Burke cannot anticipate claim 17 or any of its dependent claims.

With respect to the rejection of claim 20, Applicant respectfully submits that Burke fails to disclose the claimed features as amended. As noted above, Burke discloses using various window algorithms including simple sliding window algorithm. All of these window techniques include either a fixed window size or fixed block size to monitor the bit error rate. See column 10 lines 23-56. Burke et al. do not disclose at least performing one of performing one of generating and clearing the E-BER alarm based on an average number of errors in a subset of

the plurality of buffers. In view of these differences, it is respectfully submitted that Burke cannot anticipate claim 20 or any of its dependent claims.

New claims 23-28 broadly recite features of the preferred embodiments. New claims 23-24 recite an additional step of changing the portion of the buffers to be monitored to a desired number of buffers. As discussed above, both Burke and Bullock references do not disclose or suggest at least the feature of changing buffers to a desired number of buffers. In fact, both of these references explicitly disclose fixed-size windows or blocks.

New claim 25 recites the first subset and the second subset having different numbers of buffers. Neither Burke nor Bullock disclose or suggest at least the feature of having two subsets of buffers with different sizes.

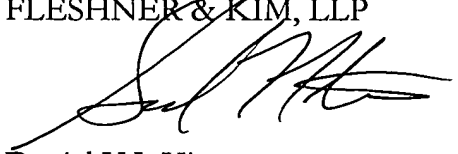
New claim 26 recites the error generation duration time and the error repairing duration time are based on a number of buffers in the first subset and the second subset respectively. Either Burke or Bullock does not disclose or suggest at least the feature of having error generation/repairing duration time based on a number of buffers in the first and the second subset. Accordingly, it is respectfully submitted that new claims 23-26 are allowable for the reasons set forth above. New claims 27-28 are depended from new claim 26, and are allowable for at least the same reasons as well as added features and the combination thereof. Therefore, it is respectfully submitted that all new claims are in condition for allowance.

CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, **Samuel W. Ntiros**, at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
FLESHNER & KIM, LLP



Daniel Y.J. Kim
Registration No. 36,186
Samuel W. Ntiros
Registration No. 39,318

P.O. Box 221200
Chantilly, Virginia 20153-1200
703 502-9440 DYK/SWN:cre
Date: January 8, 2004

Please direct all correspondence to Customer Number 34610